	Document ID	Issue Date	Pages	Title	Current OR
1	US 20040025129 A1	20040205	18	System and methods for pre-artwork signal-timing verification of an integrated circuit design	716/6
2	US 20040025123 A1	20040205	16	System and method to facilitate evaluation of integrated circuits through delay testing	716/4
3	US 20030233622 A1	20031218	84	Method and apparatus for an asynchronous pulse logic circuit	716/1
4	US 20030208723 A1	20031106	68	Automated processor generation system for designing a configurable processor and method for the same	716/1
5	US 20020073389 A1	20020613	32	Clock tuning circuit in chip design	716/6
6	US 20010047509 A1	20011129	28	Modular design method and system for programmable logic devices	716/18
7	US 6691301 B2	20040210	270	System, method and article of manufacture for signal constructs in a programming language capable of programming hardware architectures	717/114
8	US 6658628 B1	20031202	17	Developement of hardmac technology files (CLF, tech and synlib) for RTL and full gate level netlists	716/1
9	US 6611948 B1	20030826	14	Modeling circuit environmental sensitivity of a minimal level sensitive timing abstraction model	716/6
10	US 6539536 B1	20030325	69	Electronic design automation system and methods utilizing groups of multiple cells having loop-back connections for modeling port electrical characteristics	716/18

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11	US 6505339 B1	20030107	35	Behavioral synthesis links to logic synthesis	716/18
12	US 6477683 B1	20021105	39	Automated processor generation system for designing a configurable processor and method for the same	716/1
13	US 6470475 B2	20021022	9	Synthesizable synchronous static RAM	716/1
14	US 6421818 B1	20020716	80	Efficient top-down characterization method	716/18
15	US 6378123 B1	20020423	81	Method of handling macro components in circuit design synthesis	716/18
16	US 6295636 B1	20010925	82	RTL analysis for improved logic synthesis	716/18
17	US 6292931 B1	20010918	81	RTL analysis tool	716/18
18	US 6289498 B1	20010911	81	VDHL/Verilog expertise and gate synthesis automation system	716/18
19	US 6289491 B1	20010911	80	Netlist analysis tool by degree of conformity	716/5
20	US 6263483 B1	20010717	81	Method of accessing the generic netlist created by synopsys design compilier	716/18
21	US 6216257 B1	20010410	43	FPGA device and method that includes a variable grain function architecture for implementing configuration logic blocks and a complimentary variable length interconnect architecture for providing configurable routing between configuration logic blocks	716/16
22	US 6205572 B1	20010320	79	Buffering tree analysis in mapped design	716/5
23	US 6202197 B1	20010313	19	Programmable digital signal processor integrated circuit device and method for designing custom circuits from same	716/17

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24	US 6173435 B1	20010109	80	Internal clock handling in synthesis script	716/18
25	US 6152612 A	20001128	50	System and method for system level and circuit level modeling and design simulation using C++	703/23
26	US 5883814 A	19990316	20	System-on-chip layout compilation	716/2
27	US 5867399 A	19990202	64	System and method for creating and validating structural description of electronic system from higher-level and behavior-oriented description	716/18
28	US 5854752 A	19981229	20	Circuit partitioning technique for use with multiplexed inter-connections	716/7
29	US 5838954 A	19981117	85	Computer-implemented method of optimizing a time multiplexed programmable logic device	716/16
30	US 5825662 A	19981020	85	Computer-implemented method of optimizing a time multiplexed programmable logic device	716/3
31	US 5801958 A	19980901	95	Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including interactive system for hierarchical display of control and dataflow information	716/18
32	US 5761483 A	19980602	85	Optimizing and operating a time multiplexed programmable logic device	716/2
33	US 5740347 A	19980414	49	Circuit analyzer of black, gray and transparent elements	714/33

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34	US 5701441 A	19971223	85	Computer-implemented method of optimizing a design in a time multiplexed programmable logic device	716/16
35	US 5648909 A	19970715	48	Static timing verification in the presence of logically false paths	716/6
36	US 5623418 A	19970422	66	System and method for creating and validating structural description of electronic system	716/1
37	US 5579510 A	19961126	17	Method and structure for use in static timing verification of synchronous circuits	716/6
38	US 5555201 A	19960910	95	Method and system for creating and validating low level description of electronic design from higher level, behavior-oriented description, including interactive system for hierarchical display of control and dataflow information	716/1
39	US 5452239 A	19950919	131	Method of removing gated clocks from the clock nets of a netlist for timing sensitive implementation of the netlist in a hardware emulation system	703/19
40	US 5068823 A	19911126	12	Programmable integrated circuit using topological and parametric data to selectively connect and configure different high level functional blocks thereof	716/16
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